REMARKS

Status of the Application

Claims 1-20 and 39-46 are pending in the application. Claims 39-43 are withdrawn pursuant to the restriction requirement issued in the Office Action dated October 15, 2008. Claims 1-20 and 44-46 have been examined.

With this amendment, Applicant cancels withdrawn claims 39-43 and amends claims 1, 2 and 5. Applicant respectfully submits that the amended claims are fully supported by the disclosure. No new matter has been added.

After entry of this Amendment, claims 1-20 and 44-46 will be pending in the application.

Applicant respectfully requests that this Amendment be entered for purposes of appeal even if the claims as currently amended are not in condition for allowance.

Claim Rejections

Claims 1, 3, 6, and 44 — 35 U.S.C. § 103(a)

Claims 1, 3, 6, and 44 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,658,509 to Bonella *et al.* ("Bonella") in view of U.S. Pat. Pub. No. 2002/0078280 to Arimilli *et al.* ("Arimilli") and U.S. Pat. Pub. No. 2002/0069317 to Chow *et al.* ("Chow"). Applicant traverses this rejection.

Claims 1, 3 and 6 are patentable over the combination of Bonella, Arimilli and Chow for at least the reasons set forth below because, absent impermissible hindsight based on Applicant's disclosure, one of ordinary skill in the art at the time the invention was made would not have been motivated to combine the references as attempted by the Examiner.

As claimed by Applicant, a control device switches an operational mode of a ring bus from a unidirectional bus which either sends or receives a signal unidirectionally, to a bi-

directional bus which sends and receives a signal bi-directionally, when an arbitrary memory module is being removed. Applicant's invention provides continued ability to read from and write to data storage locations of remaining memory modules of the ring bus even in the absence of an arbitrary memory module.

Additionally, when an arbitrary memory module is missing from the ring bus, data which would have been written to or read from the missing memory locations is instead written to or read from a hard disk device. Thus, by providing a hard disk device for interim data storage and the dual unidirectional and bi-directional operational modes of the ring bus, Applicant's invention provides continued ability to read from and write to data storage locations even in the absence of an arbitrary memory module. The combined references do not address this problem or suggest the claimed combinations.

The primary reference, Bonella, is directed to a specialized ring bus architecture using only half as many bus lines in which, during read and write operations, half of each data word is sent from a controller in opposite directions around the ring bus passing through buffers on memory modules in the path, to be recombined to form a full data word at a buffer of a destination memory module. See column 3, lines 45-67.

Thus, each portion of ***Bonella's ring bus must always operate in a bi-directional mode*** to perform read/write operations with a target memory module. Since each half of the data word is sent in opposite directions around the ring bus, removing a memory module would remove from the ring bus architecture the buffers necessary to transmit a half data word in one of the required directions around the ring bus. A missing module would result in loss of half of each data word at the target memory module since the ring bus architecture of Bonella operates only in a bi-directional mode. Bonella, therefore, does not contemplate operation of a ring bus in a

unidirectional mode, and does not even recognize the problem solved by Applicant's invention, since Bonella's ring bus does not compensate for the missing memory module and maintain the ability to seamlessly read and write data. Further, the Examiner admits that Bonella does not disclose switching the mode of the ring bus to operate in both a bi-directional and a unidirectional mode, as required by the claim. Rather, the Examiner relies on Arimilli for teaching this feature.

Arimilli discloses first and second circuit modules, each of which has a transmitter/receiver that is selectable between a bi-directional mode that transmits and simultaneously receives via two transmission lines, and a unidirectional mode that transmits on a first transmission line and receives from a second transmission line. However, the reference says nothing with regard to operation of the circuit modules in a ring bus configuration.

Even if the circuit modules of Arimilli were used in the ring bus configuration of Bonella, the capability of Arimilli's circuit modules to switch between unidirectional mode and a bi-directional mode would not be advantageous since the ring bus of Bonella operates only in a bi-directional mode. Further, even if the Arimilli circuit module was used in the Bonella ring bus architecture, removal of an arbitrary memory module would still result in loss of data since Bonella's ring bus would still attempt to send half of each data word in opposite directions around the ring bus, with the result that half of each data word at the target memory module would be lost.

Chow does not cure the above-noted deficiencies of the Bonella-Arimilli combination. The Examiner relies on Chow to allegedly disclose a hard disk drive to which data stored in the memory modules is copied at predetermined time periods. However, Chow's system is not intended for use in a ring bus memory system. In fact, Chow teaches away from its use in a ring

bus memory system. In paragraph [0166], Chow states that an aspect of the invention is to use multiple links to couple the management module 125 to memory matrix modules 105 to form a "mesh" or "fabric type redundancy" that provides for a higher data transfer rate during normal operations. See paragraph [0166]. Chow therefore teaches away from the use of a ring bus to connect the control device to the memory modules in combination with Bonella and Arimilli.

Thus, one of ordinary skill in the art merely having knowledge of the Bonella, Arimilli and Chow references would not have been motivated to combine the references as attempted by the Examiner since, absent impermissible hindsight provided by Applicant's disclosure, the references do not suggest the combination of features as claimed by Applicant. Therefore, for at least the reasons set forth above, claim 1 is patentable over the combination of Bonella, Arimilli and Chow. Claims 3, 6 and 44 are patentable at least by virtue of their dependence.

Claims 2, 4, 5, 7, 8, 15-20, 45 and 46 — 35 U.S.C. § 103(a)

Claims 2, 4, 5, 7, 8, 15-20, 45 and 46 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella in view of Arimilli, Chow and U.S. Patent No. 5,586,291 to Lasker *et al.* ("Lasker"). Applicant traverses this rejection.

Claims 2, 4, 5, 7, 8, 15-20, 45 and 46 are patentable over the combination of Bonella, Arimilli, Chow and Lasker for at least the reasons set forth below.

Independent claims 2 and 5 contain features similar to the features recited in claim 1 and are therefore patentable over the combination of Bonella, Arimilli and Chow for reasons similar to the reasons established above for claim 1. Lasker is directed to a disk storage and cache memory system which allows faster data access by using volatile memory rather than disk storage for working data access (Abstract). Neither the portions of Lasker cited by the

Examiner, nor any other portion of Lasker, discloses or suggests the above-noted ring bus features missing in the improper combination of Bonella, Arimilli and Chow.

Accordingly, claims 2 and 5 are patentable over the combination of Bonella, Arimilli, Chow and Lasker. Claims 4, 7, 8, 15-20, 45 and 46 are patentable at least by virtue of their dependencies.

Claim 9 — 35 U.S.C. § 103(a)

Claim 9 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli and Chow, and further in view of U.S. Patent No. 6,487,623 to Emerson *et al.* ("Emerson"). Applicant traverses this rejection.

Claim 9 depends from and incorporates the features of claim 1. As established above, claim 1 is patentable over the improper combination of Bonella, Arimilli and Chow. The Examiner relies on Emerson only to allegedly disclose an FET switch as a short-circuit device for short-circuiting or opening bus connections which are disconnected by removing a memory module. Emerson discloses FET isolation buffers 160 which provide isolation of a RAM module 106 from a memory bus 105a for removal of the RAM module 106 (column 7, lines 12-25). However, the reference does not address the ring bus unidirection/bi-directional mode switching of the present invention. Thus, Emerson does not cure the deficiencies of the Bonella-Arimilli-Chow combination.

Accordingly, claim 9 is patentable over the combination of Bonella, Arimilli, Chow and Emerson since the combined references fail to disclose or suggest all of the claimed features.

Claims 10 and 11 — 35 U.S.C. § 103(a)

Claims 10 and 11 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli, Chow and Lasker, and further in view of Emerson. Applicant traverses this rejection.

Claims 10 and 11 are patentable over the combination of Bonella, Arimilli, Chow, Lasker and Emerson at least because these claims depend from and incorporate the features of claims 2 and 5, respectively, which are patentable over the improper combination of Bonella, Arimilli, Chow and Lasker, as established above. As also noted above in the arguments for claim 9, Emerson does not cure the deficiencies of the combined references.

Accordingly, claims 10 and 11 are patentable over the combination of Bonella, Arimilli, Chow, Lasker and Emerson since the combined references do not disclose or suggest all the claimed features.

Claim 12 — 35 U.S.C. § 103(a)

Claim 12 is rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli and Chow, and further in view of U.S. Patent No. 6,889,304 to Perego *et al.* ("Perego"). Applicant traverses this rejection.

Claim 12 is patentable over the combination of Bonella, Arimilli, Chow and Perego. Claim 12 depends from and incorporates the features of claim 1. As established above, claim 1 is patentable over the improper combination of Bonella, Arimilli and Chow. The Examiner relies on Perego only to allegedly disclose a connector as a short-circuit device.

However, even if Perego provides such disclosure, the reference fails to cure the deficiencies of the improper combination of Bonella, Arimilli and Chow. Accordingly, claim 12 is patentable over the combination of Bonella, Arimilli, Chow and Perego.

Claims 13 and 14 — 35 U.S.C. § 103(a)

Claims 13 and 14 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Bonella, Arimilli, Chow and Lasker, and further in view of Perego. Applicant traverses this rejection.

Claims 13 and 14 are patentable over the combination of Bonella, Arimilli, Chow, Lasker, and Perego at least because these claims depend from and incorporate the features of claims 2 and 5, respectively, which are patentable over the improper combination of Bonella, Arimilli, Chow and Lasker, as established above. As also noted above in the arguments for claim 12, Perego does not cure the deficiencies of the combined references.

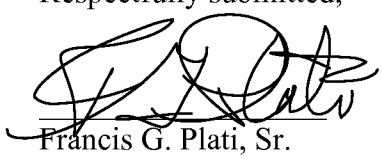
Accordingly, claims 10 and 11 are patentable over the combination of Bonella, Arimilli, Chow, Lasker and Perego since the combined references do not disclose or suggest all of the claimed features.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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